ABSTRACT OF THE DISCLOSURE

A method of manufacturing an integrated circuit (IC) utilizes a shallow trench isolation (STI) technique. The shallow trench isolation technique is used in strained silicon (SMOS) process. The liner for the trench is formed from a semiconductor or metal layer which is formed in a selective epitaxial growth (SEG) process. The SEG process can be a CVD or MBE process. Capping layers can be used above the strained silicon layer.